VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME

Related Application(s)

This application is a Divisional of U.S. Application No. 09/879,602 filed June 12, 2001 which is a Divisional of U.S. Application U.S. Application No. 09/028,807 filed February 24, 1998 now issued as U.S. Patent No. 6,246,083 on June 12, 2001. These applications are incorporated herein by reference.

Field of the Invention

The present invention relates generally to semiconductor memory devices. More particularly, it pertains to a vertical gain cell and array for a dynamic random access memory and method for forming the same.

Background of the Invention

Integrated circuit technology relies on transistors to formulate vast arrays of functional circuits and memory cells. The functional demands placed on these circuits and memory cells require the use of an ever-increasing number of linked transistors. As the number of transistors required increases, the surface space on the silicon chip/die that is allocated to each transistor dwindles. It is desirable then, to construct transistors which occupy less surface area on the silicon chip/die.

Typically, the memory cells of dynamic random access memories (DRAMs) include two main components, a field-effect transistor (FET) and a capacitor which functions as a storage element. The need to increase the storage capability of semiconductor memory devices has led to the development of very large scale integrated (VLSI) processes capable of creating smaller and smaller features. This reduction of feature size provides a substantial increase in density of memory cells in a DRAM.

The effort of extending DRAM cell density beyond the 1 gigabit generation presents the challenge of providing adequate cell capacitance within the projected cell area. Since capacitance is directly related to the surface area of the capacitor's plates, decreasing feature sizes make it very difficult to maintain sufficient cell capacitance. A cell capacitance of greater than or equal to twenty-five femto farads ($\geq$ 25 fF) is typically required in order to provide an adequate signal for sensing the stored charge over and above the anticipated noise levels. As memory cells are constructed to save precious chip space, they need to be configured in such a manner that the same data information can be stored and accessed.

An attractive means of maintaining the required storage ability is to implement a gain cell which provides an output current rather than a charge. Current sensing offers greater noise immunity and faster operation times than the conventional charge sense amplifier latch. One approach to this has been to provide a conventional, planar one transistor DRAM cell configuration to store charge on a planar diffused junction storage node. This node acts in turn as the gate of a lateral junction field-effect transistor (JFET) which is used to read the cell charge state.

An alternate approach is to construct a vertical cell with a surrounding gate write device wherein access to a read JFET is through a forward biased junction with the write bit line contact. The drawback to this method is that the forward biased junction causes the injection of minority carriers into the JFET channel which will then be collected largely by the storage node junction. Thus, the read operation of this device is destructive and transient.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a memory cell structure for dynamic random access memory devices which provide increased cell density while maintaining adequate cell capacitance and charge retention times. There is further need for such a memory cell structure offering these advantages along with a non-destructive read function.

Summary of the Invention

In one embodiment, a gain cell is provided. The gain cell includes a write transistor having multiple sides and a read transistor having multiple sides. The write transistor has a body region and first and second source/drain regions. The write transistor also has a gate that is associated with a first side of the write transistor. Similarly, the read transistor has a gate region, a body region and a first and second source/drain regions. The read transistor and the write transistor are formed in a vertical pillar of single crystalline semiconductor material the extends outwardly from a semiconductor substrate. A charge storage node surrounds a portion of the pillar adjacent to the second source/drain region of the write transistor. There is a write bit line coupled to the first source/drain region of the write transistor. A write wordline is coupled to the gate of the write transistor. A read bit line is coupled to the body region of the write transistor. And, a read wordline is coupled to second source/drain region of the read transistor.

In another embodiment, a gain cell is provided which has an n-channel transistor and a p-channel transistor. Both transistors have multiple sides. The n-channel vertical transistor has a body region and first and second source/drain regions. The n-channel transistor also has a gate that is associated with a first side of the n-channel transistor. Similarly, the p-channel transistor has a gate region, a body region and first and second source/drain regions. The n-channel transistor and the p-channel transistor are formed in a vertical pillar of single crystalline semiconductor material that extends outwardly from a semiconductor substrate. A charge storage node that surrounds a portion of the pillar adjacent to the second source/drain region of the n-channel transistor. There is a write bit line coupled to the first source/drain region of the n-channel transistor. A write wordline is coupled to the gate of the n-channel transistor. A read bit line is coupled to the body region of the n-channel transistor. And, a read wordline is coupled to second source/drain region of the p-channel transistor.

In another embodiment, a memory array on a substrate is provided. The memory array includes multiple vertical pillars of single crystalline semiconductor material extending outwardly from the substrate. The pillars have multiple sides, and each pillar includes a pair of transistors in the same pillar. Each of the transistors has a body region, a gate region and first and second source/drain regions. The second source/drain region of a first transistor comprises the gate for a second transistor. The first source/drain region of the second transistor comprises the body region of the first transistor. The pillars form an array of rows and columns. There are a number of write wordlines, wherein each write wordline is coupled to the gates of the first transistors in a row of vertical pillars in the array. A number of write bit lines are provided such that each write bit line is coupled to the first source/drain regions of the first transistors in a column of vertical pillars in the array. A charge storage node is coupled to the second source/drain region of each first transistor in the array of vertical pillars. There are also provided a number of read bit lines, such that each read bit line is coupled to the first source/drain regions of the second transistors in a row of vertical pairs in the array. A number of read wordlines are included such that each read wordline is coupled to the second source/drain regions of the second transistors in a column of vertical pillars in the array.

In another embodiment, a data storage device is provided. The data storage device includes a memory array having a plurality of gain cells. The memory array further includes multiple vertical pillars of single crystalline semiconductor material extending outwardly from the substrate. The pillars have multiple sides. Each pillar includes a pair of transistors in the same pillar. The transistors have a body region, a gate region and first and second source/drain regions. The second source/drain region of a first transistor comprises the gate for a second transistor, and the first source/drain region of the second transistor comprises the body region of the first transistor. The pillars form an array of rows and columns which also include a number of write wordlines, a number of write bit lines, a charge storage node on each pillar, a number of read bit lines, and a number of read wordlines.

Each write wordline is coupled to the gates of the first transistors in a row of vertical pillars in the array. Each write bit line is coupled to the first source/drain regions of the first transistors in a column of vertical pillars in the array. Each charge storage node is coupled to the second source/drain region of each first transistor in the array of vertical pillars. Each read bit line is coupled to the first source/drain regions of the second transistors in a row of vertical pairs in the array. And, each read wordline is coupled to the second source/drain regions of the second transistors in a column of vertical pillars in the array. A number of bit line drivers are coupled to the respective read and write bit lines. A number of wordline drivers are coupled to the respective read and write wordlines. A number of input/output controls are coupled to certain ones of the read and write bit lines and wordlines. And, a number of address decoders coupled to the read and write bit lines and wordlines.

In another embodiment, a method for reading a gain cell that includes a vertical read and a vertical write transistor formed in a single crystalline pillar of semiconductor material. The method includes receiving an address of a gain memory cell. Next, the method includes coupling a read bit line to a read wordline through the vertical read transistor, wherein a storage node on the cell acts as a gate for the vertical read transistor. Then, the method includes sensing the current that flows through the vertical read transistor.

In another embodiment, a method for fabricating a gain cell on a semiconductor substrate is provided. The method includes forming a vertical write transistor having multiple sides. The vertical write transistor is formed with a gate, a body region and first and second source/drain regions. The method includes forming a vertical read transistor having multiple sides. The vertical read transistor is formed with a body region and first and second source/drain regions. The vertical read transistor if formed having a gate region that couples to the second source/drain region of the vertical write transistor. A charge storage node is formed which couples to the second source/drain region of the vertical write transistor. A write bit

line is formed that couples to the first source/drain region of the vertical write transistor. A write wordline is formed that couples to the gate region of the vertical write transistor. A read bit line is formed that couples to the first source/drain region of the vertical read transistor. And, a read wordline is formed that couples to the second source/drain region of the vertical read transistor.

In another embodiment, a method for fabricating a gain memory cell array is provided. The method includes forming multiple pillars of semiconductor material. The multiple vertical pillars of single crystalline semiconductor material are formed extending outwardly from the substrate. The pillars are formed with multiple sides. Each pillar includes a pair of transistors in the same pillar. Each of the transistors is formed having a body region, a gate region and first and second source/drain regions. The second source/drain region of a first transistor are formed to comprise the gate for a second transistor. The first source/drain region of the second transistor is formed to comprise the body region of the first transistor. The pillars are formed in an array of rows and columns. A number of write wordlines are formed such that each write wordline is coupled to the gates of the first transistors in a row of vertical pillars in the array. A number of write bit lines are formed such that each write bit line is coupled to the first source/drain regions of the first transistors in a column of vertical pillars in the array. A charge storage node is formed that couples to the second source/drain region of each first transistor in the array of vertical pillars. A number of read bit lines are formed such that each read bit line is coupled to the first source/drain regions of the second transistors in a row of vertical pairs in the array. And a number of read wordlines are formed such that each read wordline is coupled to the second source/drain regions of the second transistors in a column of vertical pillars in the array.

These various embodiments of the vertical gain cell structure can provide increased cell density. The gain cell can be fabricated in an area as small as four lithographic features ($4F^2$). The vertical gain cell structure is capable of combination with other memory devices in order to form an array. Also, the

structure and method of fabrication yield a gain cell capable of non-destructive read operations and increased capacitance for greater data retention times.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figure 1 is a block diagram of an embodiment of a memory device including a matrix of gain cells according to the teachings of the present invention;

Figure 2 is a schematic circuit diagram of an embodiment of a gain cell according to the teachings of the present invention;

Figure 3 is a perspective view of an embodiment of a gain cell according to the teachings of the present invention; and

Figures 4A, 4B, 4C, 4D, 4E, 4F and 4G are perspective views that illustrate an embodiment of a process for fabricating an array of gain cells.

Detailed Description

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated

circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors. Also, the dimensions are representative only and not intended to be precise representations of actual manufactured structures. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

Figure 1 is a block diagram of an embodiment of a memory device 10 including a matrix or array 12 of gain cells 14 which form rows and columns according to the teachings of the invention. Each gain cell 14 comprises a vertical pillar of single crystalline semiconductor material. Each pillar includes a pair of transistors, a first transistor which performs as a write transistor and a second transistor which performs as a read transistor. In the exemplary embodiment, memory device 10 is a dynamic random access memory (DRAM). Array 12 has N rows and M columns. It is noted that N may equal M. Array 12 includes two sets of wordlines and two sets of bit lines. Within the N rows are found N rows of write wordlines WWL_0, WWL_1 . . . WWL_{N-1}, WWL_N, and there are N rows of read bit lines (data lines) RBL_0, RBL_1 . . . RBL_{N-1}, RBL_N. Each of the N rows of write wordlines is coupled to the gates of the first transistors in a row of vertical pillars in the array 12. Each of the N rows of read bit lines is coupled to the first source/drain regions of the second transistors in a row of vertical pillars in the array 12.

In analogous fashion, there are M columns. Within the M columns there are located M write bit lines WBL_0, WBL_1 . . . WBL_{M-1}, WBL_M and there are M read

wordlines RWL_0, RWL_1, . . . RWL_{M-1} , RWL_M. Each of the M write bit lines is coupled to the first source/drain regions of the first transistors in a column of vertical pillars in the array 12. Each of the M read wordlines is coupled to the second source/drain regions of the second transistors in a column of vertical pillars in the array 12. The write bit lines WBL_0 through WBL_N are used to write data into the gain cells 14 using conventional techniques. A row address is first selected and the associated write wordline goes high. Next, a write bit line is selected and data on that bit line is placed into the cell located at that intersection of the write bit line and write wordline. The write wordline next goes low, discontinuing the conduction within the gain cell 14. This act causes a charge storage node to be disconnected from the write bit line. The data is now isolated and caused to float on the charge storage node of the gain cell 14. Unlike a conventional memory device, data is read from array 12 using the read wordlines and read bit lines. To read data from a cell, either the read bit line or alternatively the read wordline is brought to a negative voltage while the other is kept at ground. A read current is subsequently produced in the gain cell 14. The magnitude of the read current is reflective of the data stored in the gain cell 14.

A write bit line driver 19 couples to the M columns of write bit lines. A read bit line driver 20 couples to the N rows of read bit lines. A write wordline driver 21 couples to N rows of write wordlines. A read wordline driver 22 couples to M columns of read wordlines. Input/output control circuits, 25, 26 and 27 respectively, control the input and output signals written to the M columns of write bit lines and read from the N rows of read bit lines or from the M columns of read wordlines respectively. Address decoders 15, 16, 17, and 18 respectively, decode incoming addresses and route data to the proper write or read bit and wordline drivers, 19, 20, 21 and 22 respectively.

<u>Gain Cell</u>

Figure 2 is a schematic circuit diagram of an embodiment of a gain cell. Each gain cell 14 includes a vertical write transistor 26, embodied as an n-channel

metal-oxide semiconductor field-effect transistor (MOSFET), and a vertical read transistor 28, embodied as a p-channel junction field-effect transistor (JFET) 28. The write transistor 26 has first and second source/drain regions 32 and 34, respectively, and a body region 36. The first source/drain region 32 is coupled to write bit line (WBL) 60. A gate of transistor 26 is formed by the write wordline (WWL) 65. The write transistor 26 has a second source/drain region 34 coupled to a storage node 110. In one embodiment of Figure 2, the charge storage node 110 is a capacitor.

The read transistor 28 has first and second source/drain regions 82 and 84, respectively, and a body region 86. The first source/drain region 82 is coupled to a read bit line 90. The second source/drain region 84 is coupled to a read wordline 95. Additionally, the second source/drain region 34 of the write transistor 26 comprises the gate of the read transistor 28. In one embodiment, the body region 36 of the write transistor 26 comprises the first source/drain region 82 of the read transistor 28. Together, the write and read transistor 26 and 28, respectively, form a vertical pillar of single crystalline semiconductor material 120, as can be seen in Figure 3.

Figure 3 is a perspective view of an embodiment of a gain cell 14 according to the teachings of the present invention. It is shown in Figure 3 that each gain cell 14 comprises a pillar 120 of single crystalline semiconductor material, having multiple sides and extending outwardly from the substrate 130. The pillar 120 consists of a vertical write transistor 26 and a vertical read transistor 28, both within the same pillar. The body region 36 of the write transistor 26 also comprises the first source/drain region 82 for the read transistor 28. Additionally, the second source/drain region 34 of the write transistor 26 comprises the gate 88 for the read transistor 28.

Figure 3 similarly illustrates the pillar's 120 structure in relation to the coupled write and read bit lines 60 and 90, respectively, as well as the write and read wordlines 65 and 95, respectively. The write bit line 60 is coupled to the first source/drain region 32 of the write transistor 26, and the read bit line 90 is coupled

to the first source/drain region 82 of the read transistor 28. The write wordline 65 is coupled to the body region of the write transistor 26 but on a second side from the read bit line 90. The remaining read wordline 95 is coupled to the second source/drain region 84 of the read transistor 28. As shown in Figure 3, a charge storage node 110 is located opposite the second source/drain region 34 of the write transistor 26. In one embodiment, the charge storage node 110 is a capacitor plate which surrounds the vertical pillar of single crystalline semiconductor material 120.

The operation of the read transistor 28 is controlled by the charge stored on the charge storage node 110. Essentially, the charge on the storage node 110 controls the conductivity of the read transistor. The conductivity of the read transistor 28 signifies a particular logic value on the charge storage node 110 of the gain cell 14. A p-n junction is formed between the second source/drain region 34 of the vertical write transistor 26 and the body region 86 of the vertical read transistor 28. This p-n junction creates a depletion zone between the second source/drain region 34 of the vertical write transistor and the body region 86 of the vertical read transistor 28.

Those skilled in the art will recognize the additional advantages to forming the pillars 120 as merged vertical pairs of write and read transistors, 26 and 28 respectively. As Figure 3 illustrates, the charge storage node 110, the write wordline 65, the read wordline 95, the charge storage node 110 and the read bit line 90 are all formed beneath the silicon surface 115. The result is a memory cell 14 which can be made in an area as small as four lithographic features ($4F^2$). Similarly, the surrounding charge storage node 110 provides increased capacitance for increased data retention time, above that found in conventional gain cells. Further, the inclusion of an independent read bit line 90 provides for a nondestructive read operation.

<u>Operation</u>

In operation, writing data to the memory cell 14 is achieved using a conventional technique. In the write mode, the write bit line 60 is brought to a

desired voltage level corresponding to "1" or "0". Next, the write wordline 65 is brought to a high voltage level, permitting conduction within the vertical write transistor 36. This action couples the logic value on the write bit line the charge storage node 110. During this sequence, the read wordline 95 is grounded. The write bit line 60 and the write wordline 65 voltage levels are limited between ground and V_{DD}.

In the read operation, either read wordline 95 or read bit line 90 is brought to a negative voltage level while the other is kept at ground. The potential difference established between the read bit line 90 and the read wordline 95 creates a readout current which corresponds to the data, or logic value, stored on the charge storage node 110. The readout current produced by the read transistor 28 is controlled by the charge present on the charge storage node 110 due to the p-n junction which exists between the second source/drain region 34 of the vertical write transistor 26 and the body region 86 of the vertical read transistor. A depletion zone is formed between these two regions. The presence of a high voltage level, or logic 1, on the charge storage node has the effect of increasing the penetration of the depletion zone into the body region 86 of the vertical read transistor.

In a standby mode, both the write wordline 65, the read wordline 95, the write bit line 60, and the read bit line 90 are all brought to ground so that the charge storage node is isolated, current flow is cut off, and the logic value on the charge storage node is kept floating.

When either the read bit line 90 or read wordline 95 is brought negative, the depletion region existing between the second source/drain region 34 of the vertical write transistor 26 and the body region 86 of the vertical read transistor 28 increases. One skilled in the art will recognize, the silicon pillar size, charge storage node shape, and impurity concentration, can be selected so as to produce the situation in which the depletion zone entirely penetrates the body region 86 and cuts off current flow between the first and second source/drain regions, 82 and 84 respectively, of the read transistor 28. Conversely, if the charge or data held by the charge storage

node 110 was a logic 0, current will still be able to flow. Hence, the conductivity of the read transistor 28 is interpreted to represent a particular logic value on the charge source node 110 of the memory cell.

Fabrication of the Gain Cell

Figures 4A-4G are perspective views illustrating an embodiment of a process for fabricating an array of gain cells. Figure 4A shows one embodiment which begins with an n-type silicon substrate wafer 200. Next, a p+ layer 150 is grown upon the n-type silicon substrate wafer 200. The p+ layer 150 is grown through epitaxial growth to a thickness of approximately 0.2 micrometers (μm). This is followed by growing a layer of p− silicon 170 on the p+ layer 156. The p− layer 170 is grown through epitaxial growth to a thickness of approximately 1.0 micrometers (μm). An n+ layer 190 is formed on the p− layer 170 by ion implantation. The n+ layer 190 has a thickness of approximately 0.15 micrometers (μm). An oxide layer 210, formed of silicon dioxide (SiO_2), is grown on the n+ layer 190. A nitride layer 220, formed of silicon nitride (Si_2N_3), is then deposited on the oxide layer 210. The nitride deposition can be performed by chemical vapor deposition (CVD).

A photoresist is applied and selectively exposed to provide a mask to define a stripe pattern in the write bit line (WBL) direction which is indicated by arrow 6000. The nitride layer 220, oxide layer 210 and n-type substrate 200 are etched through, such as by reactive ion etching (RIE), such that the n-type substrate 200 is exposed to form a first set of trenches 230. The structure is now as shown in Figure 4A.

Figure 4B shows the structure after the next sequence of steps. Trenches 230 are filled with an oxide 240. The oxide 240 may be deposited through any suitable process, such as CVD. Next, the oxide 240 is etched back to leave at a point above the lower p-n junction by approximately 0.2 micrometers. A pad oxide 245, approximately 10 nanometers (nm) in thickness, is thermally grown on the exposed walls of the trenches 230. Intrinsic polysilicon 250 is deposited by CVD to fill the trenches 230. The intrinsic polysilicon 250 is etched back through a process such as

reactive ion etching to recess it to approximately 0.3 micrometers below the p-n junction formed between the n+ layer 190 and the p- layer 170. A nitride layer 260 is deposited by CVD to fill the remaining portion of the trenches 230. The nitride 260 is planarized such as by the process of chemical-mechanical polishing/planarization (CMP). An oxide cap layer 270 is deposited on the nitride layer 260 by CVD. The thickness of the oxide cap layer 270 is approximately 50 nanometers. The structure is now as shown in Figure 4B.

Figure 4C illustrates the structure after the next sequence of steps. A photoresist is applied and selectively exposed to create a mask to define a stripe pattern in the write wordline (WWL) direction, as indicated by arrow 6050. The cap oxide 270 and nitride 260 are etched to a sufficient depth to expose the pillar 120 of single crystalline semiconductor material. The intrinsic polysilicon 250 is left covered. The single crystalline silicon pillar 120 is selectively etched to reach the p+ layer 150. The photoresist is removed such as by conventional photoresist stripping techniques. A pad oxide layer is thermally regrown on the exposed walls of the pillars 120 where it was removed in the above etching steps. The remaining nitride 260 is directionally etched in the write wordline (WWL) direction, as indicated by arrow 6050, using the cap oxide 270 as a mask. The remaining nitride is etched through to the point where the underlying intrinsic polysilicon 250 is exposed. Next, the intrinsic polysilicon 250 is isotropically etched using an etchant known in the art to selectively attack only the intrinsic polysilicon 250. All of the intrinsic polysilicon 250 is removed through etching, leaving a nitride bridge 260 across the pillars 120. A timed isotropic oxide etch is performed to remove all exposed thin oxide 245 from the walls of the pillars 120. The isotropic oxide etch leaves the thick oxide 240 at the bottom of the trenches 230. Arsenic (As) or phosphorus (P) doped glass 280 is deposited, such as by CVD, in the trenches 430 as a dopant source. The doped glass 280 is deposited to a thickness of approximately 60 nanometers. The doped glass 280 is reactive ion etched (RIE) to leave on the walls of the pillars 120 only. The structure is now as shown in Figure 4C.

Figure 4D shows the structure after the completion of the next sequence of steps. The trenches 230 are filled with a photoresist, which is then etched back to a level approximately 0.1 micrometers above the bottom of the nitride bridge 260. The doped glass is isotropically etched to remove the doped glass 280 from the top of the walls of the pillars 120. The photoresist is next removed using conventional processes. The doped glass that still remains on the walls of the pillars 120 serves as a source of dopant which is diffused into the walls of the pillars 120 to form an n+ region 34. The residual doped glass is then removed by isotropic etching. A dielectric insulator 290 is formed on the walls of the pillars 120 opposite the n+ region 34. The dielectric insulator 290 can be formed either through deposition in a CVD process or, in an alternative embodiment, it may be grown such as by thermal oxidation. Next, a charge storage node 110 is formed in the trenches 230. The charge storage node 110 is deposited by chemical vapor deposition, planarized and etched back to a level even with the bottom of the nitride bridge 260. In one embodiment, the charge storage node 110 is formed of n+ polysilicon. In another embodiment, the charge storage node 110 is formed from any other suitable refractory conductor. The structure is now as illustrated in Figure 4D.

Figure 4E illustrates the structure after the next sequence of process steps. This sequence begins with etching to strip the remaining dielectric insulator 290 from the walls of the pillars 120. A nitride layer is formed, such as through the process of CVD. The nitride layer is formed to a thickness of approximately 20 nanometers. The nitride layer is directionally etched to leave only on the vertical walls of the trenches 230. An oxide layer 310 is thermally grown on the exposed charge storage node 110. The nitride layer is then stripped away using conventional processes. An oxide layer 320 is thermally grown on the walls of the pillars 120. A write wordline 65 is deposited by a process such as CVD. In one embodiment, the write wordline 65 is formed of n+ polysilicon. The write wordline 65 is formed to a thickness of equal to or less than one-third the minimum lithographic dimension (the feature size "F"). The write wordline 65 is directionally etched to leave the write

wordline 65 on the walls of the pillars 120. The structure is now as shown in Figure 4E.

Figure 4F illustrates the structure after the next series of steps in the fabrication process. A nitride layer 330 is deposited by chemical vapor deposition (CVD). The nitride layer 330 fills the space in the trenches 230 between the write wordlines 65 and is then planarized by such a process as chemical-mechanical planarization/polishing (CMP). A photoresist is applied and selectively exposed to provide a mask which defines strips along the write wordline 65 direction. The mask covers a wordline 65 on a first side of each of the walls of the pillars 120. The nitride layer 330 is directionally etched to a sufficient depth to expose the tops of the write wordline 65. The etching may be performed by any suitable process, such as RIE. The exposed write wordline 65 is selectively etched to remove that write wordline 65. The photoresist is then removed by conventional techniques. An oxide layer 340 is deposited and planarized to fill the space of the removed wordline 65. The oxide layer 340 is directionally etched to recess the oxide layer to expose the p- layer 170. A read bit line 90 is deposited by, for example, CVD in the recesses. In one embodiment, the read bit line 90 is formed of p+ polysilicon. The read bit line 90 is etched below the top p-n junction, formed at the top of the pillar 120 between the n+ 190 and the p- layer 170. An oxide layer 350 is deposited by, for example, CVD to cap the read bit line 90. The oxide layer 350 is planarized , by for example CMP, stopping on nitride layer 330. The structure is now as illustrated in Figure 4F.

Figure 4G illustrates a perspective view of the completed structure following the next sequence of steps. The remaining nitride 330 has been stripped with an isotropic wet etch. The isotropic wet etch can be performed through the use of phosphorus acid. The write wordline 65 is then etched to recess the write wordline 65 below the top surface of the pillar 120.

Conclusion

It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The above structures and fabrication methods have been described, by way of example, not by way of limitation, with respect to the transistors, gain memory cell, memory cell array and memory device. However, the scope of the invention includes any other integrated circuit applications in which the above structures and fabrication methods are used. Thus, the scope of the invention is not limited to the particular embodiments illustrated and described herein. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.